Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**UNIVERSITY**

(Karunya Institute of Technology & Sciences)

(Declared as Deemed-to-be University under Sec.3 of the UGC Act, 1956)

**Supplementary Examination – June – 2017**

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| **Code :** | **14CS2005** | **Duration :** | **3hrs** |
| **Sub. Name :** | **COMPUTER ARCHITECTURE** | **Max. marks :** | **100** |

**ANSWER ALL QUESTIONS (5 x 20 = 100 Marks)**

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| Q. No. | Sub Div. | Questions | Course  Outcome | Marks |
| 1. | a. | What, in general terms, is the distinction between computer organization and computer architecture? | CO 2 | 4 |
| b. | List and briefly define the main structural components of a processor. | CO 1 | 6 |
| c. | Explain the various stages of instruction cycle with suitable diagram. | CO 2 | 10 |
| (OR) | | | | |
| 2. | a. | Illustrate with a figure the program flow control with and without interrupts. | CO 3 | 15 |
| b. | List and briefly define two approaches to dealing with multiple interrupts. | CO 2 | 5 |
| 3. | a. | What is the general relationship among access time, memory cost,and capacity? | CO 2 | 5 |
|  | b. | Differentiate direct mapping, associative mapping, and setassociative mapping. | CO 2 | 15 |
| (OR) | | | | |
| 4. | a. | Consider an 8 bit data 10011001 to be stored into memory. Assume that the third data bit is suffering from error and changing from 0 to 1. Compute the hamming code and syndrome word for this data and prove that the third data bit is affected by error. | CO 3 | 15 |
|  | b. | What are the differences among EPROM,EEPROM,and flash memory? | CO 2 | 5 |
| 5. | a. | List and briefly define three techniques for performing I/O. | CO 2 | 5 |
|  | b. | Explain the programmed and interrupt driven I/O techniques with a neat sketch. | CO 2 | 15 |
| (OR) | | | | |
| 6. | a. | Explain the Booth’s algorithm with suitable flowchart and also compute the product of 6 and -3. | CO 3 | 20 |
| 7. | a. | Illustrate various addressing modes with suitable diagram. | CO 3 | 15 |
|  | b. | Explain the zero address, one address, two address and three address instruction formats with suitable examples. | CO 2 | 5 |
| (OR) | | | | |
| 8. | a. | What general roles are performed by processor registers? | CO 2 | 5 |
|  | b. | Enumerate the requirements placed on the processor. | CO 3 | 7 |
|  | c. | Write short notes on user visible registers. | CO 2 | 8 |
|  | | **Compulsory**: |  |  |
| 9. | a. | Discuss the different pipeline hazards with necessary examples and explain the methods of resolving the data hazards. | CO 3 | 15 |
|  | b. | Explain the branch penalty in instruction pipeline with suitable examples. | CO 3 | 5 |

ALL THE BEST